REMARKS

Applicants respectfully request entry of this Preliminary Amendment prior to the first Official Action and prior to calculating the fees for the application.

Applicants respectfully request consideration and allowance of claims 1-32.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to deposit account No. 23-1123.

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

By: _____

Joseph R. Kelly, Reg.No. 34,847
Suite 1600 - International Centre
900 Second Avenue South
Minneapolis, Minnesota 55402-3319
Phone:(612) 334-3222 Fax:(612) 334-3312

JRK:slg

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	: Judy L. Westby et al.	
Filed	: Herewith	Group Art Unit: ---
For	: METHOD AND APPRATUS FOR USING DATA PROTECTION CODE FOR DATA INTEGRITY IN ON-CHIP MEMORY	Examiner: ---
Docket No.:	S104.12-0061	

CLAIM STATUS AND SUPPORT

Express Mail No. EV178025325US
Date of Deposit: November 26, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. (Pending) A communications channel system for using fibre-channel cyclic-redundancy code (CRC) for data integrity in an on-chip memory comprising:

a first channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel;

an on-chip frame memory located on-chip in the first channel node that receives a frame and the received frame's associated CRC from the communications channel; and

an integrity apparatus that uses the received associated CRC for data-integrity checking of the received frame that is in the on-chip frame memory.

2. (Pending) The system according to claim 1, further comprising:

a magnetic-disc-storage drive operatively coupled to the first channel node; and

a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node in a fibre-channel loop in order to transfer data between the first and second channel nodes through the fibre-channel arbitrated-loop communications channel.

3. (Pending) The system according to claim 1, further comprising:

an off-chip memory operatively coupled to the on-chip frame memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the cyclic-redundancy code while moving the received frame from the on-chip memory to the off-chip memory.

4. (Pending) The system according to claim 3, wherein the integrity apparatus checks and strips away the cyclic-redundancy code while moving the received frame to the off-chip memory, the system further comprising:

a parity-generation circuit that generates and appends parity to the data as the data are moved from the off-chip memory to the on-chip memory.

5. (Pending) The system according to claim 3, wherein a data frame devoid of a cyclic-redundancy code is held in the off-chip memory, the system further comprising:

a CRC generator that generates cyclic-redundancy code based on the data frame from the off-chip memory as the data frame is moved into the data-frame buffer, and that places the CRC into the on-chip frame memory with the data frame; and

a transmitter that transmits the data frame, including the generated cyclic-redundancy code, onto the communications channel.

6. (Pending) The system according to claim 3, wherein a received frame transferred to the on-chip frame memory from the communications channel is stored in the on-chip frame memory with CRC but without parity information.

7. (Pending) The system according to claim 3, wherein a data frame that is to be transmitted is transferred to the on-chip frame memory from the off-chip memory and is stored in the on-chip frame memory with parity but without CRC information.

8. (Pending) The system according to claim 7, wherein a received data frame transferred to the on-chip frame memory from the communications channel is stored in the on-chip frame memory with CRC but without parity information.

9. (Pending) A disc drive comprising:

a rotatable disc;

a transducer in transducing relationship to the rotating disc;

a channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel, the channel node operatively coupled to the transducer to communicate data;

an on-chip frame memory located on-chip in the channel node that receives a frame and the received frame's associated CRC from the communications channel; and

an integrity apparatus that uses the received associated CRC for data-integrity checking of the received frame that is in the on-chip frame memory.

10. (Pending) The disc drive according to claim 9, further comprising:

an off-chip memory operatively coupled to the on-chip frame memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the cyclic-redundancy code while moving the received frame from the on-chip memory to the off-chip memory.

11. (Pending) A communications method comprising steps of:

(a) supporting a fibre-channel arbitrated-loop communications channel on each of a first port and a second port of a first channel node;

(b) receiving a frame from the communications channel, the received frame including a cyclic-redundancy code that is based on other data in the received frame;

(c) storing the received frame, including the cyclic-redundancy code, into a frame buffer;

(d) moving the received frame to a memory that is separate from the frame buffer; and

(e) checking the received frame for accuracy by verifying the cyclic-redundancy code (CRC) while moving the received frame to the separate memory.

12. (Pending) The method according to claim 11, wherein the receiving step (b) further includes a step of:

(b)(i) checking the received frame for accuracy by verifying the cyclic-redundancy code while receiving the received frame from the communications channel.

13. (Pending) The method according to claim 11, further comprising a step of:

(i) transferring data through the fibre-channel arbitrated-

loop communications channel between a magnetic-disc-storage drive that is operatively coupled to the first channel node and a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node by the communications channel.

14. (Pending) The method according to claim 11, further comprising steps of:

(f) placing a frame that is to be transmitted into an on-chip frame buffer;

(g) generating the cyclic-redundancy code based on data in the frame to be transmitted; and

(h) transmitting the frame to be transmitted, including the cyclic-redundancy code, onto the communications channel.

15. (Pending) The method according to claim 14, wherein the placing step (f) further includes steps of:

(f)(i) generating parity for data of the frame to be transmitted;

(f)(ii) adding parity to the data of the frame to be transmitted; and

wherein the moving step (d) further includes a step of

(d)(i) stripping away the cyclic-redundancy code while moving the received frame to the separate memory.

16. (Pending) A communications channel system comprising:

a channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel;

a buffer that receives, from the channel node, a frame that

includes a cyclic-redundancy code;

an off-chip memory separate from the buffer;

means for moving the received frame from the buffer to the off-chip memory and checking the received frame for accuracy by verifying the cyclic-redundancy code (CRC) while moving the received frame to the off-chip memory.

17. (Pending) The system according to claim 16, wherein the means for moving further includes means for stripping away the CRC as the frame is checked and moved to the off-chip memory.

18. (Added) A system comprising:

a first serial device having n ports, each port supporting a serial communications path that carries, a data protection code within data transmissions on the serial communications path;

an on-chip memory located in the first serial device that receives a packet and the received packet's associated data protection code from the serial communications path; and

an integrity apparatus that uses the received, associated data protection code for data-integrity checking of the received packet that is in the on-chip memory.

19. (Added) The system according to claim 18 wherein n comprises one or more.

20. (Added) The system according to claim 18, further comprising:

a data storage device operatively coupled to the first serial device; and

a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device in a serial communications path in order to

transfer data between the first and second serial devices through the serial communications path.

21. (Added) The system according to claim 18, further comprising:

an off-chip memory operatively coupled to the on-chip memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the data protection code while moving the received packet from the on-chip memory to the off-chip memory.

22. (Added) The system according to claim 21, wherein the integrity apparatus checks and strips away the data protection code while moving the received packet to the off-chip memory, the system further comprising:

a data protection code generation circuit that generates and appends a second data protection code to the data as the data are moved from the off-chip memory to the on-chip memory.

23. (Added) The system according to claim 21, wherein a data packet devoid of a data protection code is held in the off-chip memory, the system further comprising:

a data protection code generator that generates data protection code based on the data packet from the off-chip memory as the data packet is moved into a data-packet buffer, and that places the generated data protection code into the on-chip memory with the data packet; and

a transmitter that transmits the data packet, including the generated data protection code, onto the communications path.

24. (Added) A data storage device, comprising:

a storage medium;

a serial device having n ports, each port supporting a serial communications path, each serial communications path carrying a data protection code within data transmissions on the serial communications path, the serial device operatively coupled to the storage medium to communicate data;

an on-chip memory located on-chip in the serial device that receives a packet and the received packet's associated data protection code from the serial communications path; and

an integrity apparatus that uses the received associated data protection code for data-integrity checking of the received packet that is in the on-chip memory.

25. (Added) The data storage device according to claim 24, further comprising:

an off-chip memory operatively coupled to the on-chip memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the data protection code while moving the received packet from the on-chip memory to the off-chip memory.

26. (Added) A method comprising:

supporting a serial communications path on each of n ports of a first serial device;

receiving a packet from the serial communications path, the received packet including a data protection code that is based on other data in the received packet;

storing the received packet, including the data protection code, into a buffer;

moving the received packet to a separate memory that is separate from the buffer; and

checking the received packet for accuracy by verifying the data protection code while moving the received packet to the separate memory.

27. (Added) The method according to claim 26, wherein receiving further comprises:

checking the received packet for accuracy by verifying the data protection code while receiving the received packet from the communications path.

28. (Added) The method according to claim 27, further comprising:

transferring data through the serial communications path between a data storage device that is operatively coupled to the first serial device and a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device by the serial communications path.

29. (Added) The method according to claim 27, further comprising:

placing a packet that is to be transmitted into an on-chip buffer;

generating the data protection code based on data in the packet to be transmitted; and

transmitting the packet to be transmitted, including the data protection code, onto the serial communications path.

30. (Added) The method according to claim 29, wherein placing comprises:

generating parity for data in the packet to be transmitted;

adding the parity to the data in the packet to be transmitted; and

wherein moving comprises:

stripping away the data protection code while moving the received packet to the separate memory.

31. (Added) A system comprising:

a serial device having n ports, each port supporting a serial communications path, each serial communications path coupling a data protection code within data transmissions on the serial communications path;

a buffer that receives, from the serial communications path, a packet that includes a data protection code;

an off-chip memory separate from the buffer;

means for moving the received packet from the buffer to the off-chip memory and checking the received packet for accuracy by verifying the data protection code while moving the received packet to the off-chip memory.

32. (Added) The system according to claim 31, wherein the means for moving further comprises:

means for stripping away the data protection code as the packet is checked and moved to the off-chip memory.

SUPPORT FOR ADDED CLAIMS

Claim 18 is supported by the specification at col. 3, line 26-31; col. 4 lines 46-55; col. 5 lines 5-19; col. 8, lines 32-36; col. 17, lines 20-61; col. 31, lines 41-57; and original claim 1.

Claim 19 is supported by col. 29 line 21; col. 31, line 20 and original claim 1.

Claim 20 is supported by col. 5, lines 47-55; col. 32, lines 22-32 and original claim 2.

Claim 21 is supported by col. 5, lines 19-25; col. 31, lines 58-64; and original claim 3.

Claim 22 is supported by col. 5, lines 25-31; col. 31, line 65; col. 32, line 3; and original claim 4.

Claim 23 is supported by col. 5, lines 31-46; col. 32, lines 4-13; and original claim 5.

Claim 24 is supported by col. 5, line 48; col. 6, line 4; col. 32, lines 31-50; and original claim 9.

Claim 25 is supported by col. 6, lines 4-9; col. 32, lines 50-56; and original claim 10.

Claim 26 is supported by col. 6, lines 11-23; col. 32, line 57; co. 33, line 5; and original claim 11.

Claim 27 is supported by col. 6, lines 36-40; col. 33, lines 1-25; and original claim 12.

Claim 28 is supported by col. 6, lines 41-43, col. 33, lines 31-29; and original claim 13.

Claim 29 is supported by col. 6, lines 23-36; col. 31, lines 1-39; and original claim 14.

Claim 30 is supported by col. 6, lines 23-36; col. 31, lines 1-39; and original claim 15.

Claim 31 is supported by col. 6, lines 48-62; col. 31, lines 40-58; and original claim 16.

Claim 32 is supported by col. 6, lines 62-65; col. 31, lines 40-58; and original claim 17.

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

By _____

Joseph R. Kelly, Reg.No. 34,847
Suite 1600 - International Centre
900 Second Avenue South
Minneapolis, Minnesota 55402-3319
Phone:(612) 334-3222 Fax:(612) 334-3312

JRK:slg